UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,394	03/12/2004	Win-Harn Liu	3313-1131P	6038

				EXAMINER
2292	7590	12/14/2006		DALEY, CHRISTOPHER ANTHONY

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ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/798,394	LIU ET AL.
	Examiner	Art Unit	
	Christopher A. Daley	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>12 March 2004</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-13</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-13</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>3/12/2004</u> is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All · b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-13 are pending.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1-4,7-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu

(US7047348).

4.   As to claim 1, Wu discloses A method of accessing PCI bus data via a debug

card, comprising:

Accessing to data of the PCI bus via a PCI interface of the debug card (Figure 2

illustrates a system comprising a PCI Interface 111 of debug card that interfaces with

the PCI bus 10, COL. 5, lines 4 – 12);

 storing the data in a buffer of the debug card (PCI Register block 20 comprise said

function, COL. 5, lines 1-3);

controlling the access to the data stored in the buffer of debug card by means of a data

control chip of the debug card (The controller SMB controller 112 performs said

function, COL. 4, line 65 – COL. 5, line 3);

storing the data in a buffer of the data control chip (Figure 2 illustrates said buffer in

element , data buffer 113, COL. 5, lines 28 – 32); and

extracting the data stored in the buffer of the data control chip via a host interface of

the debug card (Data extraction is enabled by controller, COL. 4, line 65 – COL. 5, line

3).

5.   As to claim 2, Wu discloses   The method, wherein extracting the data stored in

the buffer of the data control chip via a host interface of the debug card further

comprising: transferring the data stored in the buffer of the data control chip to the host

(Figure 2 illustrates the data flow between the host interface 114, the controller 112, and

the data buffer 113, COL. 5, lines 30-35); and

analyzing the data stored in the host (The system analyze the command type,

read/write, COL. 3, lines 5-7).

6.   As to claim 3, Wu teaches means of a data control chip of the debug card further

comprising: initializing the data control chip (Figure 2 illustrates receiving a signal from

the SMB interface to engage the controller device, COL. 3, lines 1-7);

if the data control chip is in an idle status, setting the data control chip (Figure 2

illustrates a status signal that drive the slave controller to engagement, COL. 4, lines

49-57); and

if the data control chip is not in an idle status, accessing to the PCI bus data stored in

the debug card according to the settings of the data control chip (Figure 1 illustrates

the data flow exchange with said slave controller engaged, COL.4, lines 51 – 57).

7.　　　As to claim 4, Wu discloses the method, wherein initializing the data control chip

further comprising: performing a synchronization setting of the data control chip and

debug card;

　　setting an operating mode of the data control chip (Status signal performs said function

　　as slave controller engages PCI master, COL. 5, lines 1-3);

　　 selecting a register address in the data control chip and writing an access control code

　　therein (Said function via the SMB interface, COL2., lines 25-30);

　　setting a data access width of the data control chip (Data command comprises data

　　width, COL. 2, lines 30 – 35); and

　　clearing the buffer of the debug card (It is well known in the art of clearing the buffer to

　　conserve memory usage).

8.　　　As to claim 7, Wu discloses the method, wherein if the data control chip is not in

an idle status, accessing to the PCI bus data according to the settings of the data

control chip means accessing to the PCI bus data according to a control code

stored in a register of the data control chip (Figure 2 illustrates the interaction with

controller and said elements driven by control code, COL.2, lines 30 – 47).

9.   As to claim 8, Wu discloses a debug card device, comprising: a PCI interface

operable as a connecting interface with a PCI bus (Figure 2, PCI master element 111);

    a storage module for storing PCI bus data; and

    a data control chip operable to control the access and transmission of PCI bus data,

the data control chip including: an access control module for controlling data access

according to a control signal (SMB slave controller 112);

    a transmission control module for controlling data transmission according to a control

signal (SMB slave controller 112);

    a data storage module for storing PCI bus data obtained from the debug card (PCI

register block 20);

    a register for storing an access control command (SMB slave controller 112 comprises

said register); and

     a host interface operable as an interface with a host (SMBUS interface 114).

10.   As to claim 9, Wu discloses the debug card device of claim 8, further being

connected to a host via a host interface, wherein the host comprising: a host interface

operable as a connecting interface with the debug card (Figure 2 illustrates said

interface in element 114, Col. 4, lines 60 – 67);

     a data access module operable to control the access of the PCI bus data in the data

control chip of the debug card (Figure 2, element 113, Col. 5, lines 29 – 32);

     a driving module providing an access control firmware program (Slave controller of

 Figure 2 comprises said control firmware, COL. 5, lines 1 – 3); and

a data storage module for storing extracted PCI bus data (Figure 2, element 20, COL.

5, lines 25 – 30).

11.   As to claim 10, Wu discloses the debug card device, wherein the storage

module is a buffer of the debug card (Register block 20 of Figure 2 comprises said

function, COL. 5, lines 5 – 10).

12.   As to claim 11, Wu discloses the debug card device, wherein the data storage

module is a buffer of the data control chip (Data buffer 113 of Figure 2 comprises said

buffer).

Claim Rejections - 35 USC § 103

13.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

14.   Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu

in view of Tsai et al (US6751754) hereinafter Tsai.

15.   As to claim 5, Wu does not explicitly disclose the method, wherein if the data

control chip is in an idle status setting the data control chip further comprising: setting a

data access mode of the data control chip;

 determining a data access situation of the debug card and performing counting;

setting an amount of data to be accessed each time; and

ending the idle status.

the method, wherein if the data control chip is in an idle status setting the data control

chip further comprising: setting a data access mode of the data control chip;

setting an amount of data to be accessed each time (The data byte captures said

information, COL. 2, lines 25 – 35).

Wu does not explicitly disclose determining a data access situation of the debug

card and performing counting

However, Tsai teaches determining a data access situation of the debug card

and performing counting (Figure 2 illustrates the time sequencing of events related to

the debugging process, comprising access and counting, COL. 3, lines 46 – 64. It

would have been obvious to one of ordinary skill in the art at the time of the invention to

use the single step process of Tsai in the system of Wu as it allows real time inspection

of the bus progress by elongating the cycle, COL. 1, lines 57 – 67. One of ordinary

skill in the art would have been motivated to use the single step process of Tsai in the

system of Wu as it allows real time inspection of the bus progress by elongating the

cycle, COL. 1, lines 57 – 67); and

ending the idle status (Figure 2 illustrates the engagement of the slave controller via

the address lines).

16.   As to claim 6, Tsai discloses the method, wherein ending the idle status further

comprising preparing to perform a next data access (Figure 2 illustrates the address 2

progression, COL. 2, lines 60 – 67).

17.   Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Wu in view of Tsai, and in further view of Landry et al (US6732301) hereinafter Landry.

18.   As to claims 12 and 13, Wu as modified by Tsai does not disclose   the debug

card device, wherein the host interface is a USB interface.

However, Landry teaches the debug card device, wherein the host interface is a USB

interface as illustrated in Figure 1. It would have been obvious to one of ordinary skill in

the art at the time of the invention to use the USB interface of Landry in the system of

Wu/Tsai to afford the capability to support the USB bus system, COL. 2, lines 7 – 28.

One of ordinary skill in the art would have been motivated to use the USB interface of

Landry in the system of Wu/Tsai to afford the capability to support the USB bus

system, COL. 2, lines 7 – 28.

Conclusion

19.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Christopher A. Daley whose telephone number is 571

272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

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system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CAD
12/11/2006

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